(19) Europäisches Patentamt
Europ an Patent Office
Office européen des brevets

(11) Publication number : **0 617 465 A1**

# (12) EUROPEAN PATENT APPLICATION

(21) Application number : **94302013.1**

(22) Date of filing : **22.03.94**

(51) Int. Cl.[5] : **H01L 23/498**, H01L 23/24, H01L 23/057, H01L 23/13

(30) Priority : **23.03.93 JP 63737/93**

(43) Date of publication of application : **28.09.94 Bulletin 94/39**

(84) Designated Contracting States : **DE FR GB**

(71) Applicant : **SHINKO ELECTRIC INDUSTRIES CO. LTD.**
**711, Aza Shariden,**
**Oaza Kurita**
**Nagano-shi, Nagano 380 (JP)**

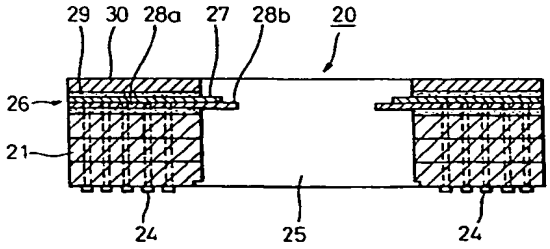
(72) Inventor : **Akagawa, Masatoshi, c/o Shinko Elec.Ind.Co.Ltd.**
**711, Aza Shariden,**
**Oaza Kurita**
**Nagano-shi, Nagano (JP)**

(74) Representative : **Rackham, Stephen Neil**
**GILL JENNINGS & EVERY,**
**Broadgate House,**
**7 Eldon Street**
**London EC2M 7LH (GB)**

## (54) A semiconductor device and package.

(57) A semiconductor-device package (20) includes a printed circuit board (21) which has a chip-accommodating hole (25) in its centre and which has external connection terminals (24) formed on one side and a flexible substrate (26) which has a supporting film (27) having a central hole aligned with the chip-accommodating hole (25). A circuit pattern (28) is formed on the supporting film (27) and inner leads (28b) project inside the central hole (25) to form micro patterns. The flexible substrate (27) is bonded on the other side of the printed circuit board (21) and an electrical connection is formed between its circuit pattern (28) and that of the circuit board (21).

Fig.1




EP 0 617 465 A1

The present invention relates to a semiconductor-device package and a semiconductor device.

A TAB (Tab Automated Bonding) tape comprises a heat resistant support film (for example, a polyimide film or the like) and a circuit pattern made of copper foil formed on the support film, the circuit pattern having inner leads projecting inside an element-accommodating hole of the support film and outer leads projecting outside the support film.

A conventional bonding technique using this TAB tape makes it possible to facilitate tests of semiconductor elements (chips) before packaging them, to simultaneously bond a narrow-pitch chip whose pitch width is so narrow that this chip cannot be simultaneously bonded by means of a conventional multi-pin and wire-bonding technique. Furthermore such a TAB tape bonding technique is superior to wire-bonding technique with regard to its high frequency properties and is suitable to high density packaging. Therefore, such a TAB tape bonding technique is very appropriate to a multi-pin, narrow-pitch and high-speed chip, such as a CPU chip or the like.

However, in such a conventional TAB tape bonding technique, both inner lead bonding and outer lead bonding is required and, as a result, a large number of working man-hours are inevitably required. In addition to this, because of requirements for mounting the package on a substrate, the pitch width between outer leads cannot be made narrow in the same manner as the pitch width between inner leads and, for this reason, the outer leads must project beyond its support film. Thus, according to such a conventional TAB tape bonding technique, the overall size of a semiconductor device typically becomes larger when a chip is mounted on it, which is contrary to demands of miniaturization.

Furthermore, when such a conventional TAB tape bonding technique is applied to a high-power chip such as a CPU chip or the like, complex and expensive packaging is necessary because adaptation to a heat radiating structure is difficult to obtain.

According to this invention a semiconductor device package comprises a printed circuit board having a chip-accommodating hole, respective surfaces and a circuit pattern, one of said surfaces being provided with external connection terminals electrically connected to said circuit pattern;

a flexible substrate comprising a supporting film having a central hole substantially in alignment with said chip-accommodating hole and a circuit pattern formed on said supporting film, at least a part of said circuit pattern projecting inside said central hole as inner leads having micro patterns; and

said flexible substrate being bonded to the other surface of said printed circuit board in such a manner that the circuit pattern of the flexible substrate is electrically connected to the circuit pattern of said printed circuit board.

Preferably a semiconductor-device comprises: a package in accordance with the invention, and a semiconductor chip bonded and mounted on said inner leads of said package, and sealing means for sealing said semiconductor chip located in said chip accommodating hole.

Preferably the semiconductor device also includes a heat radiating plate attached to said package so as to cover said chip-accommodating hole and directly or indirectly contact said semiconductor chip to support it.

According to a semiconductor-device package of this invention, it is possible to perform bonding by a conventional bonding technique in order to electrically connect said semiconductor-device package and a chip together. Thus a semiconductor-device package of the present invention is especially suitable for packaging a multi-pin and narrow-pitch chip which cannot be bonded by a conventional wire-bonding technique. Furthermore, the present invention can provide a miniature and low-cost semiconductor-device package which has excellent packaging ability because the semiconductor-device package of the present invention has no outer leads projecting outward in contrast to a TAB tape.

Furthermore, according to a semiconductor device of the present invention, it becomes possible to provide a semiconductor device which excels in heat radiating ability, high-density packaging ability and electrical properties even when it mounts a multi-pin, narrow-pitch and high-power chip.

Particular embodiments in accordance with this invention will now be described and contrasted with the prior art with reference to the accompanying drawings; in which;

Figure 1 is a vertical cross-sectional view of anembodiment of a semiconductor-device package according to the present invention;

Figure 2 is a bottom view of the example of Fig. 1;

Figure 3 is a longitudinal sectional view of the example of Fig. 1 which is completed as a semiconductor device.

Figure 4 shows another example of the substrate in the embodiment shown in Fig. 1;

Figure 5 shows another example of the heat sink in the embodiment shown in Fig. 1;

Figure 6 is a cross-sectional view of another embodiment of a semiconductor-device package of this invention;

Figure 7 is a cross-sectional view of another embodiment of a semiconductor-device package of this invention;

Figure 8 is a cross-sectional view of another embodiment of a semiconductor-device package of this invention;

Figure 9 is a cross-sectional view of an embodiment similar to that of Fig. 6; and

Figure 10 is a cross-sectional view of a semiconductor device having a conventional heat-radiating structure.

Figure. 10 shows an example of a heat radiation structure on a conventional semiconductor device.

This conventional semiconductor device has complex and expensive package structure. As shown in this figure, a circuit pattern for a PGA (Pin Grid Array) type package 10 and a chip 11 are connected through a TAB tape 12 and are sealed by a cap 13. Moreover, by means of soldering or the like, a heat sink 15 is fastened to a support 14 bonded to the chip 11.

Fig. 1 is a cross-sectional view of an embodiment of a semiconductor-device package 20 and Fig. 2 is a bottom view of the same. A multi-layer printed circuit board is indicated at 21. The top pattern and the bottom pattern of this printed circuit board are electrically coupled together through conducting portions as through-hole plating or the like. This printed circuit board has multiple layers which include a signal circuit pattern, as well as a ground circuit pattern, a power-supply circuit pattern and the like which are separated from the signal layer in view of these electrical properties. These circuit patterns are formed inside the printed circuit board.

External connection bumps or terminals 24 are formed on the bottom surface of the printed circuit board 21. These bumps 24 may be lead pins, solderable pads or conductive adhesive.

A chip-accommodating hole 25 is formed in the centre portion of the printed circuit board 21.

The printed circuit board 21 is provided on the bottom surface thereof with a dent along the periphery of the chip-accommodating hole 25. This dent works as a recess for a cap fitting.

A flexible substrate is indicated at 26. This substrate is fixed on the upper surface of the printed circuit board 21 by means of an adhesive. In the embodiment shown in Fig. 1, by etching a copper foil on the bottom surface of the supporting film 27 (for example, a polyimide film), a circuit pattern 28a on a bottom surface of the supporting film 27 and a pattern of inner leads 28b projecting inside said chip-accommodating hole 25 are formed.

The supporting film 27 is also formed in a frame-like form which has a hole in its centre portion. This hole is made so as to have a smaller size than that of the chip-accommodating hole 25. Preferably, a portion of the supporting film 27 projects inside the chip accommodating hole 25 and supports the base portions of the inner leads 28b which project inside the chip accommodating hole 25.

As described above, the flexible substrate 26 is fixed on the printed circuit board 29 by means of an adhesive.

In the same way as an electrical connection between the lower and upper patterns in a conventional printed circuit board, a circuit pattern on the upper surface of the printed circuit board 21 and the circuit pattern 28a on the bottom surface of the supporting film 27 are electrically coupled together through a plated film on the inner surface of through-holes.

This plated film is formed by boring holes through the printed circuit board at necessary points and by forming a through-hole plated film on the inner surface of the through-holes. That is to say, the whole structure of a package body 20 is able to be made by means of a substantially same structure and method as those used for a conventional printed circuit board. Furthermore, according to this embodiment, only the inner leads 28b of the circuit pattern on the top layer of the printed circuit board project inside the chip accommodating hole 25 in the form of TAB tape. This makes the structure of the package 20 different from that of a conventional semiconductor-device package.

It is preferable to bond a spacer 30 made of a material such as a resin containing a glass-filler to the upper side of the supporting film 27 by using an adhesive material. Preferably, this spacer 30 has such a thickness that the upper surface of a semiconductor chip 31 (Fig. 3) can be flush with the upper surface of the spacer 30 when the semiconductor chip 31 is mounted on the inner leads 28b.

Fig. 3 shows an embodiment of a semiconductor device in which the semiconductor chip 31 is mounted and sealed on the above-mentioned package 20.

The chip 31 can be mounted on the inner leads 28b by simultaneous bonding. The upper surface of the chip 31 mounted in this manner is almost flush with the upper surface of the spacer 30. The upper side of the chip 31 and the upper side of the spacer 30 are applied with an adhesive 33 and a heat sink 32 is fixed on these surfaces and is laid over the chip-accommodating hole 25.

The heat sink 32 may be made of a metal material such as aluminum, copper-tungsten alloy, copper and the like. A fin member 35 is preferably mounted on the heat sink 32.

Then, after the bottom surface of the chip-accommodating hole 25 is air-tightly sealed by a cap 34, a semiconductor device is completed.

Furthermore, each of the upper and bottom surfaces of the inner leads 28b can be provided with the above mentioned supporting film 27 (Fig. 4) and, as a result, the inner leads 28b can be supported from their both the upper and bottom surfaces, which reinforces the mechanical strength of the inner leads. In this case, by the formation of through-holes piecing the printed circuit board 21, the electrical coupling between the circuit pattern 28a and the circuit pattern on the upper side of the printed circuit board 21 can be established in the same manner as described above.

Furthermore, it is not always necessary to use

the spacer 30. When the spacer 30 is not used, it is preferable to use the heat sink 32 having a recess whose depth is equal to the thickness of the chip 31, as shown in Fig. 5.

Fig. 6 shows another embodiment of a semiconductor-device package of this invention. In this embodiment, the cap 34 is not used to air-tightly seal the bottom surface of the chip-accommodating hole 25, but the chip-accommodating hole 25 is filled with a resin 37 to hermetically seal the chip 31 and the TAB tape.

In an embodiment shown in Fig. 7, the chip accommodating holes 25b of the printed circuit boards 21b are larger than the chip accommodating holes 25a of the printed circuit boards 21a. Thus, chip 31 is electrically connected to the conductive patterns 39 on the circuit board 21a by bonding wires 41. Such a connection can be done by a conventional wire-bonding process.

Fig. 8 shows another embodiment of a semiconductor-device package which is similar to that of Fig. 7, except that the cap 34 is not used, but the chip-accommodating hole 25a, 25b is filled with a resin 37 in the same manner as the embodiment of Fig. 6.

Fig. 9 shows another embodiment of a semiconductor-device package which is similar to that of Fig. 6, except that the heat sink 32 and the fin member 35 are not used. Therefore, the structure and the function of this embodiment are quite the same as the embodiment of Fig. 6 except for the heat radiation means.

According to a semiconductor-device package of this invention, it is possible to bond a semiconductor device package and a chip together by a conventional TAB bonding technique in order to electrically couple the package and the chip together. Thus a semiconductor-device package of the present invention is especially suitable for packaging a multi-pin and narrow-pitch chip which cannot be bonded by a conventional wire-bonding technique. Furthermore, the present invention can provide a miniature and low-cost semiconductor-device package which has excellent packaging ability because the semiconductor-device package of the present invention has no outer leads projecting outward in contrast to a TAB tape.

According to the present invention, it becomes possible to provide a semiconductor-device which excels in heat radiating ability, high-density packaging ability and electrical properties even when it mounts a multi-pin, narrow-pitch, high-speed and high-power chip.

## Claims

1. A semiconductor-device package (20) comprising:

a printed circuit board (21) having a chip-accommodating hole (25), respective surfaces and a circuit pattern, one of said surfaces being provided with external connection terminals (24) electrically connected to said circuit pattern;

a flexible substrate (26) comprising a supporting film (27) having a central hole substantially in alignment with said chip-accommodating hole (25) and a circuit pattern (28) formed on said supporting film (27), at least a part of said circuit pattern (28) projecting inside said central hole as inner leads (28b) having micro patterns; and,

said flexible substrate (26) being bonded to the other surface of said printed circuit board (21) in such a manner that the circuit pattern (28) of the flexible substrate (26) is electrically connected to the circuit pattern of said printed circuit board (21).

2. A semiconductor-device package according to claim 1, wherein said printed circuit board (21) is multi-layer printed circuit board.

3. A semiconductor device comprising:

a package (20) in accordance with claim 1 or 2;

a semiconductor chip (31) bonded and mounted on said inner leads (28b) of said package (20); and,

sealing means (34, 37) for sealing said semiconductor chip (31) located in said chip accommodating hole (25).

4. A semiconductor-device according to claim 3, which also includes:

a heat radiating plate. (32) attached to said package (20) so as to cover said chip-accommodating hole (25) and directly or indirectly contact said semiconductor chip (31) to support it.

5. A semiconductor-device according to claim 4, wherein said heat radiating plate (32) is attached to said package (20) via a spacer (30).

6. A semiconductor-device according to claim 4 or 5, wherein said sealing means includes a cap (34) which hermetically closes said chip-accommodating hole (25) in cooperation with said heat radiating plate (32).

7. A semiconductor-device according to claim 3, 4 or 5, wherein said sealing means is a moulded resin (37) filling said chip-accommodating hole (25).

Fig.1

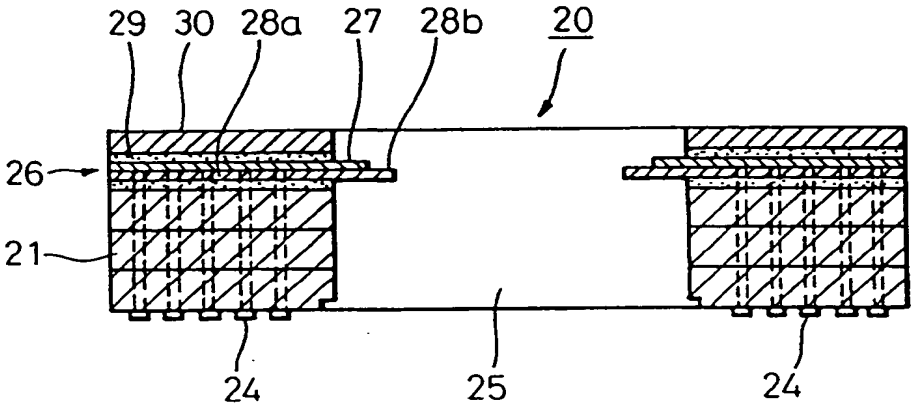



Fig.2

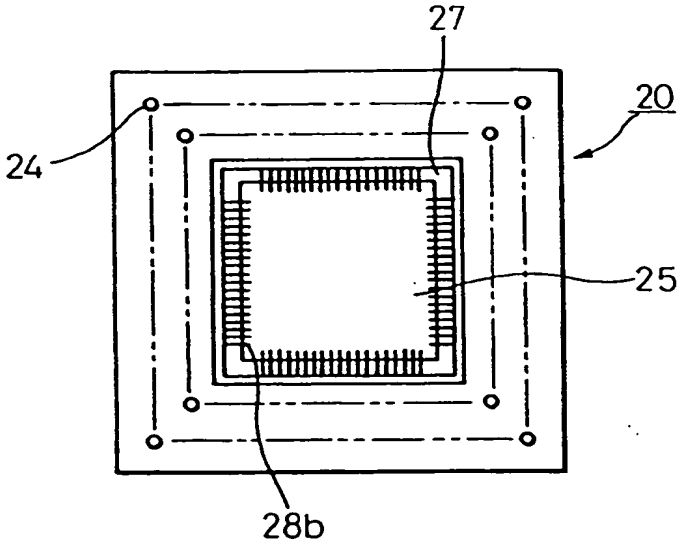


Fig.3

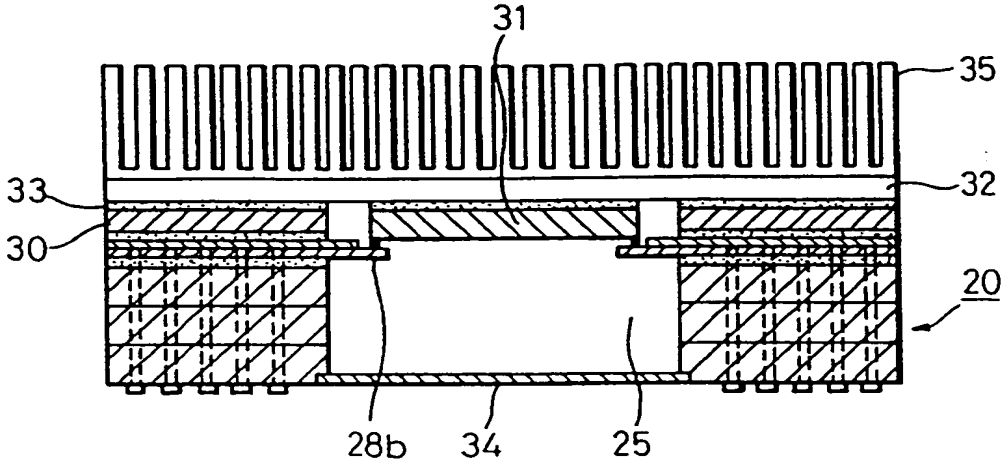



Fig.4

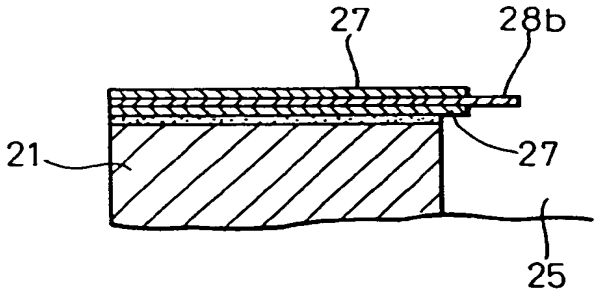



Fig.5

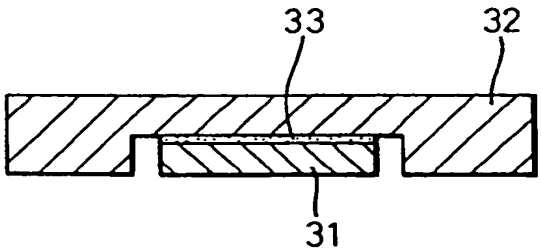


Fig.6

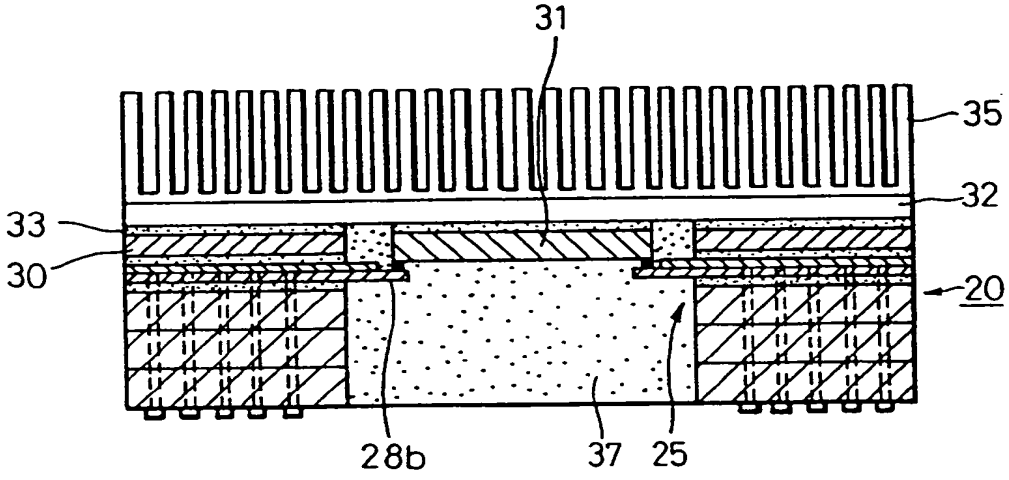



Fig.7

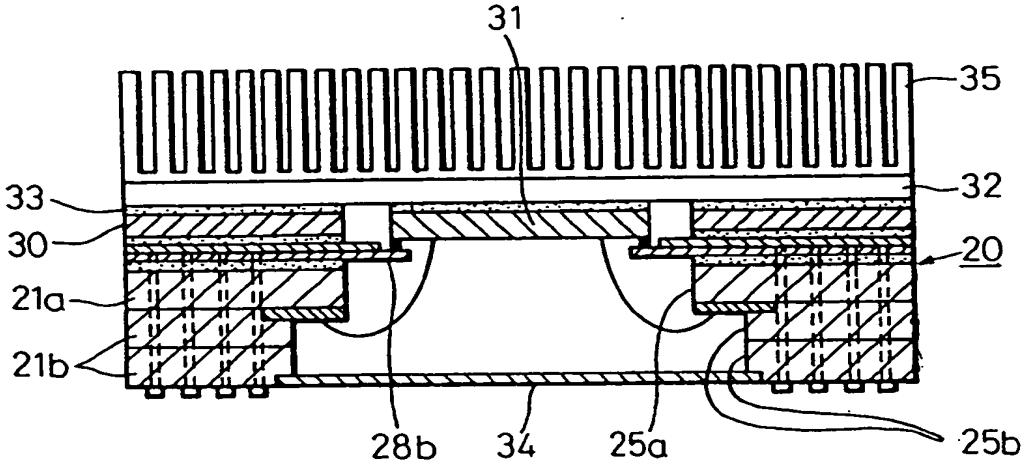


Fig.8

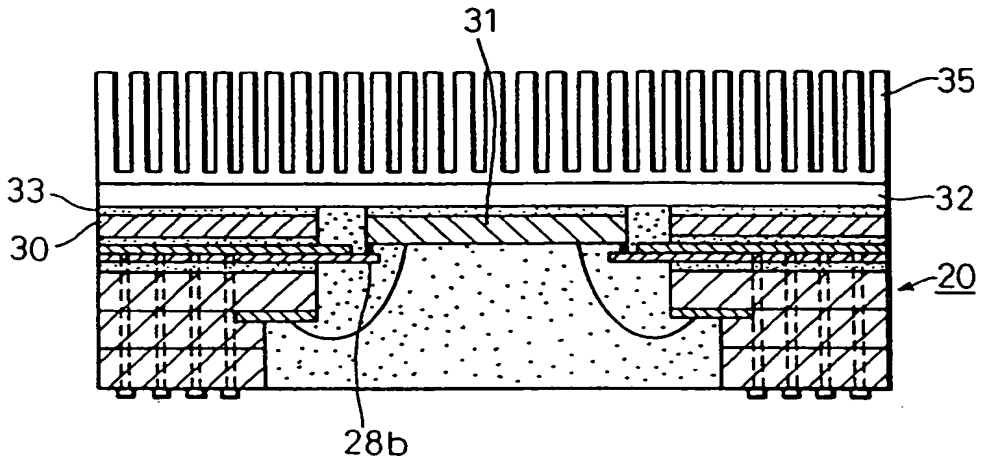



Fig.9

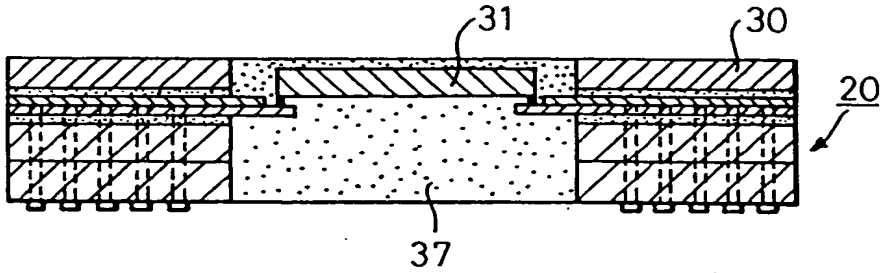
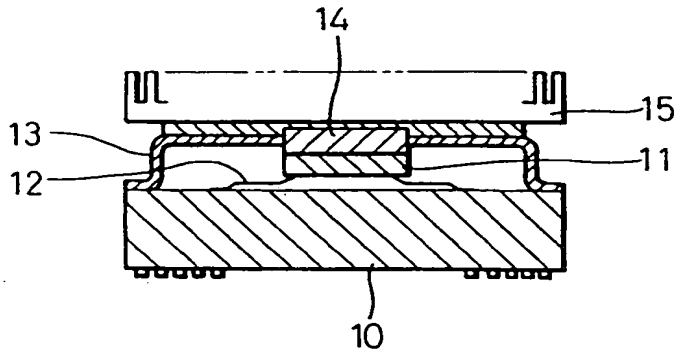


Fig.10
PRIOR ART



European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 94 30 2013

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.5) |
|---|---|---|---|
| Y | EP-A-0 352 429 (IBM)<br>* claim 1; figure 2 * | 1 | H01L23/498<br>H01L23/24 |
| A | | 4 | H01L23/057<br>H01L23/13 |
| Y | EP-A-0 524 761 (AM. T & T)<br>* column 6, line 41 - line 57; claim 6 * | 1 | |
| A | | 3,7 | |
| A | EP-A-0 476 971 (NGK)<br>* figures 1,10 * | 1-3,6 | |
| A | EP-A-0 376 062 (ETA) | | |
| A | IBM TECHNICAL DISCLOSURE BULLETIN<br>vol. 31, no. 4 , September 1988 , NEW YORK<br>pages 279 - 280<br>'tape automated bonding/pin grid array package' | | |

| TECHNICAL FIELDS SEARCHED (Int.Cl.5) |
|---|
| H01L |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 1 June 1994 | De Raeve, R |

EPO FORM 1503 03.82 (P04C01)

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document